T. Y. B. Tech
Electronics and Telecommunication Engineering

Semester - V

Sr. No.	Course Code	Course Title	L	T	P	S	Cr	Category
01	ET-25001	Digital Signal Processing	2	0	2	1	3	PCC
02	ET-25002	Configurable Logic design	3	0	2	2	4	PCC
03	ET-25003	Electromagnetic Waves and Antennas	3	0	0	1	3	PCC
04	ET(PE)-25001 ET(PE)-25002	**Program Specific Elective-I:** a) Digital Image Processing and Applications b) Information Theory and Coding	3	0	2	1	4	PEC
05	OEC-25009	Sensors and Actuators	2	0	0	1	2	OE
06	ET-25004	Internship	--	--	--	--	1	OJT
07	ET-25005	Project Stage - I	0	0	4	2	2	Project
08	ET(MDM)-25001	Multidisciplinary Minor	3	0	2	1	4	MDM
		Total	**13**	**00**	**12**	**08**	**23**	

Semester - VI

Sr. No.	Course Code	Course Title	L	T	P	S	Cr	Category
01	PCC-11	Power electronics and drives	3	0	2	1	4	PCC
02	PCC-12	Embedded system design	2	0	2	1	3	PCC
03	PCC-13	Data Communication and Networking	2	0	2	1	3	PCC
04	PCC-14	VLSI design	3	0	2	1	4	PCC
05	PEC-02	Program Specific Elective a) AI and Machine Learning b) Fiber Optic Communication	3	0	2	1	4	PEC
07	Project-02	Project Stage – II	0	0	4	2	2	Project
08	MDM-03	Multidisciplinary Minor	3	0	2	1	4	MDM
		Total	**16**	**00**	**16**	**09**	**24**	

Program Elective Courses (PECs)

Sr. No.	PEC/Sem	Option 1 Signal Processing	Option 2 Electronic Communication
01	PEC - 1/V	Digital Image Processing and Applications	Information Theory and Coding
02	PEC - 2/VI	AI and Machine Learning	Fiber Optic Communication
03	PEC - 3/VII	Digital Audio Processing	Microwave Theory and Techniques/ ASIC Physical Design
04	PEC - 4/VIII	MOOC Courses offered by NPTEL/SWAYAM	
05	PEC - 5/ VIII	MOOC Courses offered by NPTEL/SWAYAM	
06	PEC - 6/ VIII	MOOC Courses offered by NPTEL/SWAYAM	

Multidisciplinary Minor

BIS Standards for AI

Sr. No.	Semester	Course Code	Course Title	L	T	P	S	Cr
01	IV	MDM-01	Standardization – Basic Concepts	3	0	0	1	3
02	V	MDM-02	Artificial Intelligence – Basic Concepts	3	0	2	1	4
03	VI	MDM-03	Challenges for standards formation in AI	3	0	2	1	4
04	VII	MDM-04	National and International standards in AI	3	0	0	1	3
			Total	**10**	**00**	**08**	**05**	**14**

Interdisciplinary Minor

AI and ML in Signal Processing

Sr. No.	Semester	Course Code	Course Title	L	T	P	S	Cr
01	III	ID M-01	Signal Transforms	2	0	2	1	3
02	IV	ID M-02	Image and Video processing	3	0	2	1	4
03	V	ID M-03	Introduction to AI & ML techniques	3	0	2	1	4
04	VI	ID M-04	Computer vision and Pattern Recognition	3	0	2	1	4
05	VII	ID M-05	Deep learning algorithms for Signal processing	2	0	2	1	3
			Total	**13**	**00**	**10**	**05**	**18**

Honors

Wireless Communication and Next Generation Networks

Sr. No.	Semester	Course Code	Course Title	L	T	P	S	Cr
01	III	H-01	Random Signal and Stochastic Process	2	1	0	1	3
02	IV	H-02	Advance in Digital Communication	3	0	2	1	4
03	V	H-03	Cognitive Radio	3	0	2	1	4
04	VI	H-04	Software Defined Networks	3	0	2	1	4
05	VII	H-05	Next Generation Technologies	2	0	2	1	3
			Total	**13**	**01**	**08**	**05**	**18**

Digital Signal Processing

Teaching Scheme
Lectures: 2 hrs/week

Examination Scheme
Midsem: 30 marks
Teachers Assessment: 20 marks
End-Sem Exam- 50 marks.

Course Outcomes:

At the end of this course students will demonstrate the ability to

1. Interpret, represent and process discrete/digital signals and systems.
2. Analyze discrete time signals in frequency domain.
3. Learn Discrete Fourier and Fast Fourier Algorithms and their different versions.
4. Design IIR filters for processing of discrete time.
5. Design FIR filters for processing discrete time.
6. Application of Digital Signal Processing Algorithms for providing solutions for social cause.

Unit 1 **(6hrs)**

Structures for Discrete Time Systems: Block Diagram representation and Signal Flow Graph representation of Linear Constant Coefficient Difference EQUATION, Basic Network Structures for FIR and IIR Systems, Overview of Finite precision Numerical effects

Unit 2 **(7hrs)**

IIR Filter Design: Concept of analog filter design (required for digital filter design), Design of IIR filters from analog filters, IIR filter design by approximation of derivatives, , IIR filter design by impulse invariance method, Bilinear transformation method, warping effect. Characteristics of Butterworth filters, Chebyshev filters and elliptic filters, Butterworth filter design, IIR filter realization using direct form, cascade form and parallel form, Finite word length effect in IIR filter design.

Unit 3 **(7hrs)**

FIR Filter Design: Ideal filter requirements, Gibbs phenomenon, windowing techniques, characteristics and comparison of different window functions, Design of linear phase FIR filter using windows and frequency sampling method. FIR filters realization using direct form, cascade form and lattice form, Finite word length effect in FIR filter design

Unit 4 **(6hrs)**

Applications and Projects: Address recent trends in DSP algorithms (like FFT, DFT etc) with perspective of research & explore applications of DSP. Project based applications to be designed to find cost time and performance effective solutions to Local problems.

Text Books:

- S. K Mitra, "DSP a computer Based approach", MCGraw Hill

- John G. Proakis, Dimitris G. Manolakis, “Digital Signal Processing: algorithms and Applications” Fourth edition, Pearson Prentice Hall, 2007. Principles,
- A. Oppenheim and R. W. Schafer, Discrete-time Signal Processing, Pearson 2014.

Reference Book:

- Dr. Shaila Apte, "Digital Signal Processing", Wiley India Publication, second edition, 2009.
- Ifaeachor E.C, Jervis B. W., "Digital Signal Processing: A Practical approach", 2nd edition, Pearson Publication, 2002.
- K.A. Navas, R. Jayadevan, 'Lab Primer through MATLAB: Digital Signal Processing " PHI, 2014.
- Li Tan, Jean Jiang, "Digital Signal Processing: Fundamentals and applications" Academic press,2008.
- S. Salivahanan, McGraw Hill,2011. C. Gnanpriya, "Digital Signal processing”, (ET-21003) 2nd edition

Digital Signal Processing Lab

Teaching Scheme	**Examination Scheme**
Practical: 2 hrs/week	Continuous Assessment: 50 marks
	External Assessment: 50 marks.

Course Outcomes:

At the end of the course, students will demonstrate the ability to

1. Verify & demonstrate basic concepts of digital signal processing.
2. Analyze the signals in time & frequency domain.
3. Design of digital filters for specific applications.
4. Implement Multirate Signal Processing Techniques.

List of Experiments:

1. Generation of Basic Signals using C/Python and MATLAB.
2. Verification of sampling theorem.
3. Verification of linear convolution in C/Python and MATLAB using two finite sequences.
4. Implementation of circular convolution in C/Python and MATLAB.
5. Find DFT for a signal & plot the spectrum.
6. Linear & circular convolution using DFT & IDFT.
7. Design a filter to remove noise from noisy signal.
8. Design of FIR filter in C/Python and MATLAB.
9. Design of IIR filter in C/Python and MATLAB.
10. Design moving average & median filter.
11. Implement up-sampling & down-sampling of signals.

Configurable Logic Design

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
Midsem: 30 marks
Teachers Assessment: 20 marks
End-Sem Exam- 50 marks.

Course Outcomes:

At the end of this course students will demonstrate the ability to:

1. Write codes for digital building blocks using Verilog HDL
2. Design Finite State Machines
3. Model the digital designs including FSMs to Processor architectures using the knowledge of HDL Language.
4. Interpret MIPS Processor
5. Use IP cores for early development of product.
6. Concept of Neuromorphic computing in VLSI.

Unit-1 **[8 Hrs]**

Hardware Description Language: HDL Fundamentals and Design entry by Verilog / System Verilog, Test benches.

Digital Building Blocks: Combinatorial and Sequential building blocks using Verilog

Unit – 2 **[10 Hrs]**

Sequential Logic Design: Top-down approach to Design, Synchronous FSM design (Mealy and Moore Machines), Static Timing analysis, Metastability, clock issues, Asynchronous FSM Design

Unit-3 **[6 Hrs]**

Data Path and Control Path Design: Unsigned multiplication, Signed multiplication, GCD computation.

Unit-4 **[8 Hrs]**

Instruction set Architecture: Machine Language, Assembly Language, MIPS instruction set, R type I type, J type instructions encoding, MIPS general purpose registers, signed unsigned instructions, floating point instructions, Addressing modes, Pseudo instructions, Exceptions, HDL representation of single cycle CPU data path and control path. Control path and Data path design of Multi cycle Processor and a Pipelined processor, Performance analysis.

Unit-5 **[4 Hrs]**

IP and Prototyping: IP in various forms: RTL Source code, Encrypted source code, soft IP, Hard IP, Physical IP, case studies. **Logic Arrays:** PAL, PLA, FPGA, SoC implementation.

Unit-6 **[4 Hrs]**

Concepts of Neuromorphic Computing in VLSI

Roadmap on neuromorphic computing and engineering, Spiking Neural Networks (SNN) in Digital Circuits, Digital Synapses, Digital Neural Models. Applications of Neuromorphic Computing in Robotics and Autonomous Systems, Health and Brain-Computer Interface (BCI), Edge AI and IoT devices, Cyber security and Anomaly Detection, Space and Aerospace. Advantages of Neuromorphic Computing, Challenges and future prospects

Text Books

1. Stephen Brown and Zvonko Vranesic, “Fundamentals of Digital logic with verilog design”, Mc-Graw hill.
2. Zainalabedin Navabi, “Verilog Digital System Design RT Level Synthesis, Testbench and Verification”, 2nd edition, 2006, Tata McGraw-Hill Edition
3. William Fletcher - An Engineering Approach to Digital Design, PH
4. David Harris and Sarah Harris, “Digital Design and Computer Architecture”, 2nd edition, 2013, Morgan Kaufmann
5. Douglas Smith, “HDL Chip Design: A Practical Guide for Designing, Synthesizing & Simulating ASICs & FPGAs Using VHDL or Verilog”, Doone publications.
6. David A. Patterson, John Hennessy, “ Computer Organization and Design”, ELSEVIER, Morgan Kaufmann
7. IEEE standard HDL based on Verilog HDL, published by IEEE.

Configurable Logic Design Lab

Teaching Scheme
Practical: 2 hrs/week

Examination Scheme
Continuous Assessment: 50 marks
External Assessment: 50 marks.

Course Outcomes:

At the end of this course students will demonstrate the ability to:

1. Use Verilog HDL to implement Boolean functions, combinative and sequential functions in FPGA
2. Know the structure and operation of CPLD, FPGA and SoC.
3. Design Processor using Verilog HDL
4. Have the clear understanding of all three paradigms of implementation of digital logic circuits
   a. using fixed function ICs b. using programmable logic c. using ASIC

List of Practical

1. Verilog implementation of Mux / Demux, Full Adder, magnitude comparator, encoder / decoder, priority encoder, parity generator, Code converters, D FF, Shift registers (SISO, SIPO, PISO, bidirectional), Synchronous Counters.
2. HDL code for Sequence generator / detectors, Synchronous FSM – Mealy and Moore machines.
3. HDL code for Vending machines - Traffic Light controller, ATM, elevator control.
4. Realization of single port SRAM in Verilog.
5. HDL code for UART, SPI, I2C and Arbiter
6. HDL code for generic building blocks like decoder, adder, shifter, register file and ALU used by any micro architecture
7. HDL code for single cycle Processor data path and control path

8. HDL code for MIPS instruction memory, data memory

Electromagnetic Waves and Antennas

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
Midsem: 30 marks
Teachers Assessment: 20 marks
End-Sem Exam- 50 marks.

Course Outcomes:

At the end of the course, students will demonstrate the ability to
1. Analyze the transmission lines and estimate voltage and current at any point on transmission line for various load conditions.
2. Use the Smith Chart as a tool for transmission line calculations and analysis.
3. Determine the solution to the real-life plane wave problems for various boundary conditions using concepts of electromagnetic wave propagation.
4. Analyze the field equations for the wave propagation in special cases such as lossless, low loss and lossy dielectrics medium.
5. Visualize TE and TM mode patterns of field distributions in rectangular waveguide.
6. Characterize the radiation of an antenna and antenna array in terms of pattern, directivity, gain, bandwidth and radiation resistance.

Unit 1 **(9hrs)**
Transmission Lines: Introduction, Concept of distributed elements, Equations of voltage and current, standing waves and impedance transformation, Lossless and low loss transmission lines, Power transfer on a transmission line, Analysis of transmission line in terms of admittances, Transmission line calculations with the help of Smith chart, Applications of transmission line, Impedance matching using transmission lines.

Unit 2 **(7hrs)**
Uniform Plane Waves: Maxwell’s equations. Homogeneous unbound medium, Wave equation for time harmonic fields, Solution of the wave equation, Uniform plane wave, Wave polarization, Wave propagation in conducting medium, Phase velocity of a wave, Power flow and Poynting vector.

Unit 3 **(7hrs)**
Plane Waves at Media Interface: Plane wave in arbitrary direction, Boundary conditions, Plane wave at dielectric interface, Reflection and refraction of waves at dielectric interface, Total

internal reflection, Wave polarization at media interface, Brewster angle, Fields and power flow at media interface, Reflection from conducting boundary.

Unit 4 **(6hrs)**

Guided Waves: Waves in Parallel plane waveguide: Transverse Electric (TE) mode, transverse Magnetic (TM) mode, Cut-off frequency, Phase velocity and dispersion. Transverse Electromagnetic (TEM) mode, Analysis of waveguide-general approach, Waves in Rectangular waveguides.

Unit 5 **(7hrs)**

Antennas: Introduction to Antenna basics and characteristics, Effective aperture, Friis Transmission formula, general concept of dipole antenna. Short dipole and loop antenna, Slot antennas, Babinet's principle.

Unit 6 **(6hrs)**

Antenna Arrays: Introduction to Arrays, Two - element and N - element uniform linear arrays, Array Factor calculations, Broadside array, End fire array and Phased array.

Text Books:

• Shevgaonkar, R. K., "Electromagnetic waves", Tata McGraw-Hill Education, 2006.

• Balanis, Constantine A., "Antenna theory: analysis and design", John wiley& sons, 2016.

Reference Books:

• Nathan Ida, "Engineering Electromagnetics", 2nd Edition, Springer.

• Edward C. Jordan and Keith G. Balmain, "Electromagnetic Waves and Radiating Systems", Prentice Hall of India, 2006.

• Ramo, S., Whinnery J. R., and van Duzer. T, "Fields and Waves in Communication Electronics", 3rd Edition, John Wiley & Sons.

PEC-01 Program Specific Elective
Digital Image Processing and Applications

Teaching Scheme:
Lectures: 3 hrs/week
Self-Study: 1 hr/week
Lab 2 hrs/week

Examination Scheme:
Mid Sem Evaluation-30 Marks TA-20 Marks
End Sem Evaluation-50 Marks

Course Outcomes:
After successful completion of this course the students will be able to
1. Explain the fundamental concepts and techniques of digital image processing.
2. Apply image enhancement and restoration techniques in both spatial and frequency domains.
3. Implement image segmentation and feature extraction methods for various applications.
4. Analyse and apply appropriate image compression techniques.
5. Develop practical solutions for real-world problems using image processing algorithms.

Course contents:
- **Unit I:** Introduction to Digital Image Processing
  Fundamental steps in image processing, Image acquisition and sampling, Quantization and image representation, Applications of digital image processing
- **Unit II:** Image Enhancement Techniques
  Spatial domain methods: contrast stretching, histogram equalization, Frequency domain methods: Fourier transform, filtering, Noise reduction techniques
- **Unit III:** Image Restoration and Reconstruction
  Degradation models, Noise modelling and filtering, Inverse and Wiener filtering, Geometric transformations
- **Unit IV:** Colour Image Processing
  Colour models: RGB, HSI, CMY, Colour transformations and enhancements, Pseudo-colouring techniques
- **Unit V:** Image Segmentation and Feature Extraction
  Edge detection methods: Sobel, Prewitt, Canny, Thresholding techniques, Region-based segmentation, Feature extraction: texture, shape, and colour features
- **Unit VI:** Image Compression and Applications
  Compression techniques: JPEG, MPEG, Lossy and lossless compression, Applications in medical imaging, remote sensing, and biometrics

References:

1. "Digital Image Processing" by Rafael C. Gonzalez and Richard E. Woods, 3rd Edition, Pearson Education, 2008.
2. "Digital Image Processing" by William K. Pratt, John Wiley & Sons, 4th Edition, 2007.

List of Experiments:

1. To acquire grayscale and color images, perform basic manipulations (resize, crop), and display them using image processing software.
2. To enhance image contrast using histogram equalization and apply spatial filters like smoothing and sharpening.
3. To implement the Discrete Fourier Transform (DFT) on an image and apply low-pass and high-pass filtering in the frequency domain.
4. To simulate common noise models (Gaussian, Salt & Pepper) and apply restoration techniques such as median, Gaussian, and Wiener filtering.
5. To apply geometric operations such as scaling, rotation, translation, and affine transformation to an image.
6. To detect edges in images using gradient-based operators such as Sobel, Prewitt, and Canny edge detectors.
7. To segment images using thresholding, region growing, and morphological-based segmentation approaches.
8. To convert images between color spaces (e.g., RGB to HSI) and apply pseudo-coloring and color enhancement techniques.
9. To perform binary morphological operations such as erosion, dilation, opening, and closing for shape analysis.
10. To implement basic image compression techniques like run-length encoding and understand JPEG compression concepts.

PEC-01 Program Specific Elective
Information Theory and Coding

Teaching Scheme:	**Examination Scheme:**
Lectures: 2 Hrs/week	Internal Evaluation: 50 marks
Practical: 2 hrs/week	MSE 30, Assignment/Quiz: 20
	End-Sem Exam: 50 Marks

Course Outcomes:

At the end of the course, students will demonstrate the ability to

1. Design, implement and compare coding techniques for the memoryless and stationary discrete sources.
2. Implement binary block and convolutional channel coding techniques for error detection and correction in both forms viz. hardware and software.
3. Estimate error detection and correction capabilities of block and convolutional channel codes.

4. Explore the calculations of channel capacity to support error-free transmission using source coding and channel coding algorithms.

Contents:

Unit I: Information Measures [4 Hrs]

Discrete Source models – Memoryless and Stationary, Mutual Information, Self Information, Conditional
Information, Average Mutual Information, Entropy, Entropy of the block, Conditional Entropy, Information Measures for Analog Sources

Unit II: Coding Techniques for Discrete Sources [8 Hrs]

For Memory-less Sources: Fixed length coding, Variable length coding – Prefix codes, Kraft Inequality, Coding Techniques - Huffman, Shannon-Fano, Higher order extensions, Average code length, Coding efficiency.
For Stationary Sources: Lempel-Ziv encoder and decoder, Software implementation of these techniques
using appropriate data structures

Unit III: Coding Techniques for Analog Sources [6 Hrs]

Optimum quantization, Distortion, Measures, Rate distortion function (RDF), Distortion rate function (DRF), RDF and DRF for Gaussian Source, Upper and Lower bounds on RDF/DRF, Scalar quantization – Uniform, Non-Uniform, Vector quantization, K-means algorithm, Coding techniques taxonomy.

Unit IV: Channel Capacity and Block Codes [10 Hrs]

Channel models – Discrete and Waveform, Channel capacity, Introduction to channel coding – Code rate and Redundancy, Linear Block codes - Vector spaces and subspaces, Generator matrix, Systematic codes,
Parity check matrix, Syndrome Testing, Error Correction, Implementation of encoder and decoder, Cyclic codes – Encoding in systematic form, circuit for dividing polynomials, Systematic encoding and error detection with linear feedback shift registers.

Unit V: Error Detection and Correction Capability of Block Codes [6 Hrs]

Weight and distance of binary vectors, minimum distance of a linear code, Error detection and correction capability, Erasure correction, Usefulness of the standard array, Estimating code capability, Error detection vs. correction trade-offs, Block codes examples such as Hamming codes, Golay codes.

Unit VI: Convolutional codes [8 Hrs]

Convolutional encoding – Connection representation, State representation, Tree Diagram, Trellis Diagram, Convolutional decoding – Maximum likelihood decoding, Algorithms such as Viterbi, Sequential, Feedback, Viterbi decoder implementation, Distance properties, Minimum free distance,

Error Correction capacity, Systematic and Nonsymmetric Codes

Text Books:

- Bernard Sklar and Pabitra Kumar Ray, "Digital Communications: Fundamentals and Applications", Pearson Education Asia, Thirdd Edition
- John G. Proakis and Masoud Salehi, "Digital Communications", Tata McGraw Hill, Fifth Edition

Reference Books:

- Salvatore Gravano, "Introduction to Error Control Codes", Oxford University Press, First Edition
- Simon Haykins, "Digital Communication", Wiley, Second Edition
- B. P. Lathi, "Modern Digital and Analog Communication Systems", Oxford press, Third Edition

Information Theory and Coding Lab

Teaching Scheme:
Practical: 2 Hrs/week

Examination Scheme:
Term work: 50 marks
Oral: 50 Marks

Course Outcomes:

At the end of the lab course, students will demonstrate the ability to

1. Design and deploy various encoding and decoding techniques for discrete sources using programming languages such as C/C++.
2. Build the hardware and evaluate performance of block and convolutional encoders and decoders.

List of Assignments/Experiments:

1. Entropy computations – Average Self Information (Entropy), Conditional entropy, Average mutual information for binary and M-ary sources.
2. Design and Implement Huffman encoder and decoder for the given string.
3. Design and Implement Shannon-Fano encoder and decoder for the given string.
4. Design and Implement Lempel-Ziv-Welch encoder and decoder for the given string.

5. Build and test the performance of Linear Block Codes: Encoder and Decoder.
6. Build and test the performance of Cyclic Codes: Encoder and Decoder
7. Build and test the performance of Convolution Codes: Encoder and Decoder

NOTE: The programming is to be carried out using C, C++. The hardware implementation is to be done using digital circuits/kits available in the lab.)

Project Stage - I

[D-S-P-T: Design – Simulate – Prototype – Test]

Teaching Scheme	**Examination Scheme**
Study: 2 hr./week	Term-work: 50 Marks
Practical: 6 hrs./week	Practical: 50 Marks

Course Outcomes:

At the end of the laboratory work, students will demonstrate the ability to

1. Identify a problem statement either from a rigorous literature survey or the industry requirements analysis.
2. Design a solution for the identified problem by applying acquired technical knowledge.
3. Simulate, Develop and Test the Prototype with a standard solution/ process.
4. Learn to work in a team and coordinate within the group for timely completion of targeted work.
5. Demonstrate an ability to present their project work through a comprehensive Report and Presentation.

Guidelines:

• The mini project is a team activity having 3-4 students in a team. This is electronic product design work with a focus on electronic circuit design.

• The mini project may be a complete hardware or a combination of hardware and software.

• Mini Project should cater to a small system required in laboratory or real life.

• It should encompass components, devices, analog or digital ICs, micro controller with which functional familiarity is introduced.

• After interactions with course coordinator and based on comprehensive literature survey/ Industry requirements analysis, the student shall identify the title and define the aim and objectives of mini project.

• Student is expected to detail out specifications, methodology, resources required, critical issues involved in design and implementation and submit the proposal within first week of the semester.

• The student is expected to exert on design, development, and testing of the proposed work as per the schedule.

• Layout should be made using CAD based PCB simulation software. Due considerations should be given for power requirement of the system, mechanical aspects for enclosure and control panel design.

• Completed mini project and documentation in the form of mini project report is to be submitted at the end of semester.

• The tutorial sessions should be used for discussion on standard practices used for electronic circuits/product design, converting the circuit design into a complete electronic product, PCB design using suitable simulation software, estimation of power budget analysis of the product, front panel design and mechanical aspects of the product, and guidelines for documentation /report writing.

Sr No	Items	Description of activity
1	Scope (TRL-2)	Research Problem Identification, Literature, objective, methodology and Architecture / Plan of work
2	Student project group	Four students maximum per project. The student group remained the same till the completion of the three stages of the project. No change in topic/ group / guide is allowed in subsequent stages of projects. In case of eventuality, alternate guide may be allotted.
3	Problem statement identification	It is mandatory for faculty members to float projects with carefully selected problem statements well in advance. The project should be floated and allotted within a week after the 5th semester registration process is over. Since the project will run for one and half years, it is required by the department to float topics for the choice of students. The project topic should be in line with National Mission / Atmanirbhar bharat/ Industry requirements/ Funding body requirements / socially relevant project / Sustainable Development Goals (SDGs)
4	Project topic selection	The student group shall choose a project topic amongst the available topics given by the department based on the previous semester CGPA.
5	Self-Study material	The department should recommend relevant online / offline self-study

	for the student	materials on IPR, technical paper writing, plagiarism, safety, NDA, Regulatory standards, for example- BIS, etc.
6	End Semester Evaluation process	The end semester evaluation shall be based on projectpower point presentation andwell-structured project report. The evaluation shall be done by the panel of at least three members including one of them is project guide.

Evaluation sheet for Project-I

MIS No	Name of student	Research problem identification	Literature	Objective	Project Report	Viva Voce and presentation skill	Out of 50 marks
		10 M	10 M	10 M	10M	10M	

SEMESTER - VI

Power Electronics & Drives

Teaching Scheme:
Lectures: 2 hrs/week
Self-Study: 1 hr/week
Lab 2 hrs/week

Examination Scheme:
Mid Sem Evaluation-30 Marks TA-20 Marks
End Sem Evaluation-50 Marks

Module 1: Fundamentals and Emerging Semiconductor Devices

- Overview of Power Electronics: Scope, applications, and trends
- Review of Semiconductor Devices: Diodes, BJTs, MOSFETs, IGBTs, SCRs
- Emerging Devices:
  - Silicon Carbide (SiC) and Gallium Nitride (GaN) Devices
  - Comparison: Si vs. SiC vs. GaN
  - Thermal management and reliability aspects

Module 2: Modern Power Converter Topologies

- DC-DC Converters: Buck, Boost, Buck-Boost, Cuk, SEPIC, Zeta converters
- DC-AC Converters (Inverters):
  - Single-phase and three-phase inverters
  - PWM techniques: SPWM, SVPWM, and digital PWM
- AC-AC Converters: Cycloconverters, Matrix Converters
- Flyback Converter – Self Study

Module 3: Digital Control of Power Converters

- Microcontroller and DSP-based converter control
- Closed-loop control: PI, PID, model predictive control

Module 4: Electrical Drives and Control

- Types of Electrical Drives: DC Drives, Induction Motor Drives, Synchronous Motor Drives
- Dynamic modelling of drives
- Torque-speed characteristics
- Drives for Special Machines: BLDC, PMSM, SRM
- Stepper Motors – Self study

Module 5: Applications and Integration with Renewable Energy

- Drives for Electric Vehicles (EVs)
  - Traction inverter design, regenerative braking, motor selection
- Power electronics in solar and wind systems
  - MPPT techniques, inverter interfacing

- Smart Grids and FACTS Devices
  - STATCOM, SSSC, UPQC, and HVDC

Module 6: Applications for Industry & Railways (Self-study)

- High-efficiency DC-DC converters and battery management for battery powered railways
- Energy Storage Integration

Text Books

1. Power Electronics – M.H. Rashid
2. Fundamentals of Power Semiconductor Devices – B.J. Baliga
3. Power Electronics – Ned Mohan
4. Digital Control of HF SMPS – Corradini

Reference books

1. Modern Power Electronics and AC Drives – Bimal K. Bose
2. Power Electronics Handbook – Rashid (Editor) • Corradini et al.
3. Advanced Electric Drive Vehicles – Ali Emadi
4. Wide Bandgap Power Packaging – K. Suganuma
5. Design of Smart Power Grid Renewable Energy Systems – Ali Keyhani

POWER ELECTRONICS & DRIVES -LAB

Experiment 1: Simulation of 1-Phase Controlled Rectifier with RL Load

- Objective:
  To simulate a single-phase full-bridge controlled rectifier and analyze the output voltage waveform for RL load.
- Tools:
  MATLAB/Simulink
- Expected Output:
  Output voltage waveform with reduced average value as α increases.

Experiment 2: Simulation and Harmonic Analysis of Inverter Output

- Objective:
  To simulate a single-phase inverter and analyze the harmonics in output waveform using FFT.
- Tools:
  MATLAB/Simulink with FFT block or PSIM
- Expected Output:
  Output voltage waveform and harmonic content (THD values).

Experiment 3: Buck Converter Design and Analysis

- Objective:
  To simulate and analyze a step-down (Buck) DC-DC converter using a switching device and diode.
- Tools:
  MATLAB/Simulink or LTSpice
- Expected Output:
  Output DC voltage less than input, proportional to duty cycle.

Experiment 4: BLDC Motor Drive using Arduino

- Objective:
  To implement speed control of a BLDC motor using Arduino and observe commutation behavior.
- Tools:
  Arduino Uno, BLDC Motor with Hall Sensors, Motor Driver Module, PWM Code
- Expected Output:
  Smooth speed control and correct commutation of BLDC motor.

Experiment 5: Gate Driver Design for MOSFET/IGBT

- Objective:
  To design and test a gate driver circuit for a power MOSFET or IGBT.
- Tools:
  IR2110 or TLP250 IC, Breadboard, Oscilloscope, Signal Generator
- Expected Output:
  Clean switching waveform with appropriate gate voltage and fast transitions.

Experiment 6: SVPWM Implementation Using STM32 Microcontroller

- Objective:
  To implement Space Vector PWM to control a three-phase inverter.
- Tools:
  STM32 Nucleo board, STM32CubeIDE, 3-Phase Inverter Simulation Model (or Hardware)
- Expected Output:
  3-phase PWM waveform with 120° displacement and optimized utilization.

Experiment 7: Solar-Powered Inverter with MPPT (Simulation)

- Objective:
  To simulate a solar-powered inverter with MPPT algorithm.
- Tools:
  MATLAB/Simulink (Solar PV, Boost Converter, MPPT blocks)
- Expected Output:
  Maximum power point tracking with inverter feeding sinusoidal AC output.

Experiment 8: Harmonic Analysis Using Power Analyzer

- Objective:
  To measure and analyze harmonic content in inverter output using a power analyzer.
- Tools:
  Power Analyzer (Fluke/Yokogawa), Inverter Circuit, Oscilloscope
- Expected Output:
  Total Harmonic Distortion value, harmonic spectrum of output.

Mini/Capstone Project Topics

- Design of IoT-enabled motor drive
- SiC-based high-efficiency converter
- Design and fabrication of EV traction inverter
- Grid-tied solar inverter with battery backup
- AI/ML-based fault detection in drives

Suggested Tools & Platforms

- MATLAB/Simulink, PSIM, LTSpice, PLECS
- Arduino, STM32, TI Launchpad, dSPACE
- ANSYS for thermal/EMI simulations
- Need for PCB design-based project
- Testing and EMI/EMC

Embedded System Design

Teaching Scheme	**Examination Scheme**
Lectures:2hrs./week	TA-20 Marks
Practical:2hrs/week	Mid Sem Exam-30 Marks
Self-study:1hr/week	End Sem Exam- 50 Marks

Course Outcomes:

At the end of the course, students will demonstrate the ability to

1. Understand the internal architecture of microcontrollers and other salient features.
2. Interface digital Input and Output devices (sensors/actuators) using GPIOs and PWM blocks.
3. Utilize serial synchronous and asynchronous buses to communicate with other devices.
4. Design prototypes to monitor and automate processes from several domains.

Unit 1 **(8 hrs)**

Microcontroller architecture and Embedded Computing:

CISC and RISC architecture, Instruction Set, Basic Embedded Processor/Microcontroller Architecture and peripheral study. Introduction to Embedding Computing Applications, Challenges in Embedded System Design, Design Process.

Unit 2 **(6 hrs)**

Digital and Analog IO Interfacing:

Digital I/Os, PWM interfacing and Programming, A/D and D/A converters, Hardware and software interrupts, Timers, DEBUG interface

Unit 3 **(6 hrs)**

Communication Buses and Programming:

USART, Serial peripheral interface (SPI), Inter integrated interface (I2C), Memory interfacing, CAN Protocol, Serial communication protocols programming (Wi-Fi/Bluetooth/Zigbee)

Unit 4 **(4 hrs)**

Microcontroller case studies and Applications:

Industrial automation, Automotive, Home appliances, Consumer electronics, medical devices, Military systems, Environmental monitoring, Robotics, Internet of Things (IoT), Edge Computing.

Self-Study **(1 hr/week)**

Study of Different Integrated Development Environments, debugging and Programming software and tools, Hardware Abstraction Layer, Toolchain.

List of Recommended Books:

Text Books:

- Arm education media, Embedded system Fundamentals with Cortex-M based microcontroller by Dr Alexandar G. Dean, FRDM-KL25Z Edition
- ARM Cortex Technical Reference Manual

Reference Books:

- PACKT Publication,2016, ARM CORTEX COOKBOOK, First Edition by Dr. Mark Fisher
- Elsevier Publication, 2005 Embedded System by Raj Kamal, 2nd Ed., TATA McGraw Hill, 2009.

e Learning Resources:

https://elearn.nptel.ac.in/shop/nptel/microprocessors-and-microcontrollers-arm-cortex-m0-using-rp2040/?v=c86ee0d9d7ed

https://github.com/rust-embedded/cortex-m

How to use this book? - ESP32-C3 Wireless Adventure: A Comprehensive Guide to IoT (espressif.github.io)

Embedded System Design: Laboratory

Teaching Scheme | **Examination Scheme**
Practical: 2 hr / week | Term Work: 50 Marks
Oral/Practical: 50 Marks

Course Outcomes:

1. Interpret the datasheets related to the microcontroller and its peripherals Program and associated peripheral devices.
2. Design, develop and test applications using microcontrollers and associated peripherals.
3. Design and implement experiments with different paradigms such as Polled mode, Interrupt driven and DMA channels.

List of Experiments based on STM32xx/TI processor

Write Assembly/Embedded 'C' program for

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Capture analog readings of rotary potentiometer connected to an ADC channel.
7. Program - Read, Write and Verify - serial EEPROM using I2Cas well as SPI interface.
8. Calling C function from assembly program and vice versa.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case of microcontroller hang.
11. To develop an assembly code and C code to compute Euclidian distance between any two points
12. To develop assembly and C code for implementation of convolution operation
13. To design and implement filters in C to enhance the features of given input sequence

Data Communication and Networking

Teaching Scheme-
2 Lectures/Week, Self Study-1 hr
Credits-3

Examination Scheme-
Mid-Sem - 30 Marks
Internal Assessment- 20 Marks
End Sem Exam-50 Marks

Course Outcomes:

At the end of the course, students will demonstrate the ability to

1. Explain the fundamental underlying principles of layered network architecture.
2. Comprehend the congestion, routing protocols at various network layers.
3. Design a network considering the QOS parameters.
4. Analyze the performance of various communication protocols and networks.
5. Implement flow control and congestion in the network.
6. Illustrate the interfacing of components in the existing networks

Unit1 **(5L+1S)**

Basics of Data Communication: Introduction to Protocols and Standards,Layered Network Protocol Architectures, Internet Devices, Topology , LAN, MAN, WAN, Data Transmission – Types, Media and impairments, Data Rate and Throughput.

Unit 2 **(3L+1S)**

Data Link Layer

Framing, Flow Control, Error Control Mechanism, Error detection, Multiple Access protocols-CSMA/CA, CSMA/CD, ARP, RARP

Unit 3 **(5L+1S)**

Network Layer:

IPv4, IPv6, IP addresses and subnetting, Transitioning from IPv4 to IPv6, ICMP, IGMP, HCP, NAT, Unicast Routing Protocols

Unit4 **(3L+1S)**

Transport Layer- Connectionless transport - User Datagram Protocol (UDP), Connection-oriented transport – Transmission Control Protocol (TCP), Congestion control Mechanisms, Flow Control mechanisms, Quality of Service.

Unit5 **(5L+1S)**

Wireless Networks: Bluetooth, Zigbee, Ethernet, Wi-Fi, Wireless Sensor Network, AdHoc Networks, Circuit and Packet Switching, Software Defined Networking, Network Security

Unit6 **(3L+1S)**

Application Layer:

The Web and Hyper Text Transfer Protocol, File transfer, electronic mail, Domain Name System

Textbooks:

- J.F. Kurose and K. W. Ross, "Computer Networking – A top down approach featuring the Internet", Pearson Education, 5th Edition
- L. Peterson and B. Davie, "Computer Networks – A Systems Approach" Elsevier Morgan Kaufmann Publisher, 5th Edition.

Reference Books:

- S. Keshav, "An Engineering Approach to Computer Networking", Pearson Education.
- B. A. Forouzan, "Data Communications and Networking", Tata McGraw Hill, 4th Edition.
- Andrew Tanenbaum, "Computer networks", Prentice Hall.
- D. Comer, "Computer Networks and Internet/TCP-IP", Prentice Hall.
- William Stallings, "Data and computer communications", Prentice Hall.

Data Communication and Networking Lab

Teaching Scheme	**Examination Scheme**
Practical: 2 hrs./week	Term work - 50 Marks
	Oral – 50 marks

1) Study of Ns2 Simulator and Installation of NS2
2) Transfer of packets between two Nodes
   a) UDP b) TCP
3) To Forward packets via single router
   a) UDP b) TCP
4) To transfer packets of UDP and TCP using 4 nodes, assign color to nodes and Traffic
5) To transfer packets of UDP and TCP using 5 nodes
6) Router Broadcasting the UDP/TCP packets
7) To transfer packets of UDP and TCP using 6 Nodes
8) Queue Management

9) To transfer UDP and TCP packets on Ring Topology Network
10) Distance Vector Routing
11) Throughput and X-graph
12) To implement Dijkstra’s shortest path algorithm on NS2 (Greedy approach)
13) To determine shortest path using C/C++/Python
14) To implement sliding window protocol in C/C++/Python
15) To capture packets using Wireshark and analyze them at all the layers of network.

VLSI Design

Teaching Scheme
Lectures: 3 hrs/week

Examination Scheme
Midsem: 30 marks
Teachers Assessment: 20 marks
End-Sem Exam- 50 marks.

Course Outcomes:

At the end of this course students will demonstrate the ability to:

a) Illustrate / Infer / Interpret the importance of manufacturing process of CMOS based integrated circuits, energy band diagrams of MOS, scaling technology and the secondary effect in MOSFETs.
b) Model MOS transistors, its small geometry effects and interconnect wire for performance analysis and Evaluate impact of technology scaling on Robustness, performance, and energy/power dissipation of CMOS Inverter.
c) Design / formulate / estimate simple and complex combinatorial logic circuit for optimized area, speed, power, glitch free and reduced supply voltages.
d) Choose the right clocking scheme according to the functionality, speed and power of a circuit.
e) Build the data-path subsystem and array subsystem blocks with all the design trade-offs.
f) Understand the operation and working of Non-volatile memories

Unit-1 **[8 Hrs]**

Introduction to VLSI: Evolution of VLSI, Energy band diagram of MOS Capacitor, Operation and working of MOS Transistor, Derivation of Threshold voltage equation, Secondary effects in MOSFETS.

Technology Scaling and Road map, Scaling issues, Manufacturing process of CMOS integrated circuits: Standard 4 mask NMOS Fabrication process, packaging integrated circuits, High–k, Metal Gate Technology, FinFET, IC layout design and tools: CMOS n-well process design rules, stick diagram, ASIC Design Flow.

Unit – 2 **[7 Hrs]**

Electrical wire models: MOS capacitances, Modelling of MOS transistors using SPICE level I and II equations, BSIM Models. The ideal wire, the lumped model, the lumped RC model, the distributed RC model, the transmission line model, SPICE wire models.

Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay. CMOS inverter: Switching Threshold, Noise Margin, Dynamic behaviour of CMOS inverter, propagation delay of Inverter, RC Delay, Dynamic and Static Power consumption and Low power design criteria.

Unit-3 **[8 Hrs]**

Combinational logic: Static CMOS design, Pass transistor logic, transmission gate logic, Logic effort delay, Dynamic logic, Speed and power dissipation in dynamic logic, cascading dynamic gates, standard cell design, sizing of gates, estimating and optimizing delay in standard cell and clock distribution networks.

Unit-4 **[6 Hrs]**

Sequential logic: Timing Constraints in CMOS latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master slave edge-triggered register, Dynamic latches and registers, STA and max and min delay constraints for Flip-flop.

Unit-5 **[4 Hrs]**

Data-Path Subsystems building blocks: Case Study design discussions for Addition / Subtraction, Comparator, Counters, Shifters and Multipliers from related technical papers.

Array Subsystems: 6T/8T/10T SRAM Cell design, Row Circuitry, Column circuitry, SRAM Cell Array design discussions from technical papers.

Unit-6 **[4 Hrs]**

Introduction to Storage devices for In-Memory Computation: Overview of Mass Data Storage devices and technology, Flash Memory, Alternative Memory / Emerging Memory devices, the fundamental operating physics of various non-volatile memory (NVM) materials and devices used for neuromorphic computing, like resistive Random Access Memory (RRAM), phase change material (PCM), nano magnetic and spintronic devices, Superconducting electronic memory for Quantum Information Processing (QIP).

Text Books

- N. Weste and D. Harris, "CMOS VLSI Design A Circuits and Systems Perspective", 4th edition, Pearson.
- J M Rabaey, A. Chandrakasan, B. Nikolic, "Digital Integrated Circuits A Design Perspective", Pearson.

- Sung Mo Kang, Yusuf Leblebici, “CMOS digital integrated circuits”, TataMcGraw Hill Publication.
- Baker Li Boyce, “CMOS Circuit Design, Layout, and Simulation”, Wiley, 2nd Edition.

Reference Book

- Neil E Weste and Kamran Eshraghian, “ Principle of CMOS VLSI Design”, Pearson education

VLSI Design Lab

Teaching Scheme
Practical: 2 hrs/week

Examination Scheme
Continuous Assessment: 50 marks
External Assessment: 50 marks.

Course Outcomes:

At the end of this course students will demonstrate the ability to:

1. Interpret the behavior of MOS Transistor with the help of SPICE tools.
2. DC and Transient analysis of CMOS Inverter.
3. Physical design and Verification of CMOS Inverter.
4. Design of digital circuits, clock and buffer distribution networks for standard cell design according to design specs provided.

List of Practical

9. DC analysis of NMOS and PMOS Transistor using NGSPICE. Estimate I_{ON}, I_{OFF}, S and λ for 180nm / 130nm / 90nm channel length transistors.
10. V_{th} analysis of NMOS and PMOS Transistor using various methods.
11. DC and Transient analysis of CMOS Inverter using NGSPICE. Estimate V_{IL}, V_{IH}, V_{OL}, V_{OH}, NM_L, NM_H from DC analysis and tp_{HL}, tp_{LH} from transient analysis.
12. Design of 5 stage and 7 stage ring oscillator using NGSPICE. Estimate f_{osc}.
13. Schematic design of CMOS Inverter and its DC, Transient analysis using Cadence EDA Tool.
14. Schematic to Symbol generation using Cadence EDA Tool.
15. Schematic to Layout of CMOS Inverter using Cadence EDA Tool.
16. Post Layout simulation of CMOS Inverter and Parasitic Extraction.
17. Design of all basic gates and /or combinatorial circuits using Cadence EDA Tool.
18. Design of a 6 Transistor SRAM cell using Cadence EDA Tool. Estimate CR and PR, Read SNM and Write SNM.
19. Design of Sequential circuits like D FF, simple clock and buffer distribution networks for standard cell design using Cadence EDA Tool.

PEC-02 Program Specific Elective

AI and Machine Learning

Teaching Scheme:
Lectures: 3 hrs/week
Self-Study: 1 hr/week
Lab 2 hrs/week

Examination Scheme:
Mid Sem Evaluation-30 Marks TA-20 Marks
End Sem Evaluation-50 Marks

Course Outcomes:

After successful completion of this course the students will be able to

1. Explain the fundamental concepts and techniques of machine learning.
2. Apply supervised and unsupervised learning algorithms to real-world problems.
3. Design and implement neural network models for various applications.
4. Analyse the performance of machine learning models using appropriate metrics.
5. Develop practical solutions using machine learning tools and libraries.

Course contents:

Unit I: Introduction to Machine Learning

Definition and types of learning: supervised, unsupervised, and reinforcement learning, Applications of machine learning in various domains, Overview of the machine learning pipeline

Unit II: Supervised Learning Algorithms

Linear regression and logistic regression, Decision trees and random forests, Support Vector Machines (SVM), Evaluation metrics: accuracy, precision, recall, F1-score

Unit III: Unsupervised Learning Algorithms

Clustering techniques: K-means, hierarchical clustering, Dimensionality reduction: Principal Component Analysis (PCA), Anomaly detection methods,

Unit IV: Neural Networks and Deep Learning

Perceptron and multilayer perceptron, Backpropagation algorithm, Introduction to deep learning architectures, Convolutional Neural Networks (CNNs) basics

Unit V: Reinforcement Learning

Markov Decision Processes (MDPs), Q-learning and policy gradient methods, Applications in robotics and game playing.

Unit VI: Practical Applications and Case Studies

Implementing machine learning models using Python libraries, Case studies in image recognition, natural language processing, and recommendation systems, Ethical considerations in AI and machine learning.

References:

1. "Pattern Recognition and Machine Learning" by Christopher M. Bishop, Springer, 2006.
2. "Machine Learning: A Probabilistic Perspective" by Kevin P. Murphy, MIT Press, 2012.
3. "Introduction to Machine Learning" by Ethem Alpaydin, MIT Press, 3rd Edition, 2014. H. Stark & J. W. Woods, Probability and Random Processes with Applications to Signal Processing, 2014.

List of Experiments:

1. To clean and prepare real-world datasets by handling missing values, encoding categorical variables, and applying normalization techniques.
2. To implement linear and polynomial regression algorithms for predicting continuous variables and evaluate performance using error metrics.
3. To classify data points using the k-NN algorithm and evaluate model performance using accuracy and confusion matrix.
4. To implement logistic regression for binary classification problems and analyze the results using ROC curves.
5. To train decision tree and random forest classifiers and compare their performance on classification datasets.
6. To train linear and non-linear SVM models and visualize the decision boundary for classification tasks.
7. To implement k-means clustering for unlabeled data and determine the optimal number of clusters using the elbow method.
8. To reduce the dimensionality of data using PCA and visualize the variance explained by principal components.
9. To design, train, and evaluate a feedforward neural network using Keras for a classification task (e.g., MNIST digit recognition).
10. To develop an end-to-end machine learning application (e.g., spam detection, sentiment analysis, image classification) including preprocessing, model training, and evaluation.

PEC-02 Program Specific Elective

Fiber Optic Communications

Teaching Scheme Lectures: 3 hrs./week **Examination Scheme:**
Practical: 2 hrs./week Mid Sem Exam -30 marks
Teacher Assessment – 20 marks
End Sem Exam - 50 marks

Course Outcomes:
At the end of the course, students will demonstrate the ability to
1. Explain the principles and advantages of fiber optic communication.
2. Describe the modes propagating in optical fiber using mode theory.
3. Analyze the performance of optical sources and detectors.
4. Estimate the power and rise time budget for an optical link.
5. Illustrate the concepts and components used in WDM.
6. Design an optical network and analyse its performance.

Unit 1 **(4 hrs)**
Overview of Optical Fiber Communications: Motivations for Lightwave communications, optical spectral bands, decibel units, network information rates, key elements of optical fiber systems, Standards for optical fiber communications.

Unit 2 **(8 hrs)**
Optical Fibers: Structures Wave guiding and Fabrication: Introduction to vector nature of light, basic optical laws and definitions, optical fiber modes and configurations, Mode theory of circular waveguide, Single mode fibers, Graded index fibers, Fiber materials, Photonic crystal fibers, Fiber fabrication, Mechanical properties of fiber,

Unit 3 **(8 hrs)**
Transmission Characteristics of Optical Fiber: Attenuation, Material absorption loss, Scattering loss, Bending Loss, Dispersion, Chromatic dispersion, Intermodal dispersion, Polarization mode dispersion, Dispersion modified single mode fibers. International fiber standards.

Unit 4 **(8 hrs)**
Optical Sources, Detectors and Link Design: LEDs and Laser Diodes, Photo detectors pin-diodes, APDs, detector responsivity, noise, Optical receivers. Optical link design, Power budget and Rise Time Budget.

Unit 5 **(6 hrs)**

WDM Concepts and Components: Overview of Wavelength Division Multiplexing, Passive Optical Couplers, Isolator and Circulators, Fiber grating filters, Active optical components, Tunable light sources, Erbium Doped Fiber Amplifier, Raman Amplifier

Unit 6 **(8 hrs)**

Optical Networks: Network Concepts, Network topologies, SONET/SDH, High speed light wave links, Optical Add/Drop Multiplexing, Optical Switching, Passive Optical Networks, Optical Ethernet, Optical Fiber System performance monitoring and Measurement, Optical Time Domain Reflectometer(OTDR).

Textbooks:

- Gerd Keiser, "Fibre Optic communication", McGraw-Hill, 5th Edition, 2010
- John M Senior," Optical Fiber Communications Principles and Practice", Pearson 3rd Edition

Reference Book:

- Siva Ram Murth, Mohan Guruswamy " WDM Optical Networks Concepts Design and Algorithms" ,PHI Eastern Economy ,Edition,2001

Fiber Optic Communications Lab

Teaching Scheme:
Practical: 2 Hrs/week

Examination Scheme:
Term work: 50 marks, Oral: 50 Marks

Course Outcomes:

At the end of the lab course, students will demonstrate the ability to

1. Design and deploy various optical networks and analyses its performance.
2. Build the hardware and Measurement of fiber characteristics, fiber damage and splice loss/connector loss by OTDR.

List of Assignments/Experiments:

1. Measurement of numerical aperture of a fiber after preparing the fiber ends.
2. Study of losses in optical fiber.
3. Setting up of fiber optic digital link.
4. Preparation of splice joint and measurement of splice loss.
5. Power vs. current (P-I) characteristics and measure slope efficiency of laser diode.

6. Voltage vs. current (V-I) characteristics of laser diode.
7. Power vs. current (P-I) characteristics and measure slope efficiency of LED.
8. Voltage vs. current (V-I) characteristics of LED.
9. Characteristics of photodiode and measure the responsivity.
10. Characteristics of avalanche photodiode [APD] and measure the responsivity.
11. Measurement of fiber characteristics, fiber damage and splice loss/connector loss by OTDR.

Project Stage - II

Teaching Scheme **Examination Scheme** Term-work: 50 Marks
Practical - 16 hrs./week Oral: 50 Marks

Course Outcomes:

At the end of the laboratory work, students will demonstrate the ability to

1. Identify a problem statement from a rigorous literature survey or the industry requirements analysis.
2. Simulate and design a solution for the identified problem by applying acquired technical knowledge.
3. Develop and test the prototype/algorithm to solve the complex engineering problem.
4. Accomplish all objectives of the project in allocated period with efficient teamwork.
5. Demonstrate ability to present project work through a comprehensive report and project presentation.
6. Demonstrate professional ethics and values by solving engineering problems to benefit society or industry.

Guidelines: After interactions with project guides/industry experts, based on a comprehensive literature survey/ Industry requirements analysis, the student shall identify the title and define the aim and objectives of a project. The student is expected to work on details specifications, methodology, resources required, critical issues in design and implementation, and submit the project proposal within the first two weeks of semester. The student is expected to work on the design, development, and testing of the proposed project work as per the schedule.

Deliverables: The project report is to be submitted at the end of the semester. This report includes a summary of the literature survey, detailed objectives, project specifications, design, proof of concept, developed system/Algorithm, results, contributions, and innovations in project work.

Evaluation: A committee comprising of guide and internal evaluation panel members shall assess the progress at mid-semester. Guide and appointed external examiner shall assess the progress/performance of the student based on a report, project presentation, and Q & A. This evaluation will be conducted at the end of the semester.

Sr No	Items	Description of activity
1	**Scope (TRL-3)**	Continuation of Project-I, Planning, fabrication and development of hardware / software and execution; relevant standards.
2	**Self-Study material for the student**	The department shall recommend relevant online / offline self-study materials on Incubation, Innovation (online / offline)
3	**End Semester Evaluation process**	The end semester evaluation shall be based on project work in power point presentation and a project report. The evaluation shall be done by the panel of faculty members, at least three members including one of them is project guide.

Evaluation sheet for Project -II

MIS No	Name of student	Planning	Development of hardware / software	Experimentation	Project Report	Viva Voce and presentation skill	Out of 50 marks
		10 M	10M	10M	10M	10M	

Internship and Project (Industry/Corporate/Academia)

Teaching Scheme — Practical in Industrial/Corporate/Academia - 20 hrs./week

Examination Scheme Term-work: 50 Marks
Oral: 50 Marks

Course Outcomes:

At the end of the work, students will demonstrate the ability to

1. Explain the basic concepts of assigned internship work and Undertake problem identification, formulation and solution.
2. Implement work plan in their Industrial In-Plant Training Project work.
3. Identify a problem statement from the industry requirements analysis.
4. Simulate and Design a solution for the identified problem by applying acquired technical knowledge.
5. Develop and test the prototype/algorithm to solve the complex engineering problem.
6. Demonstrate an ability to presentproject work through a comprehensive report and project presentation.
7. Accomplish all the objectives of the project, resulting in at least a thesis publication, and research outputs in terms of publications in high impact factor journals, conference proceedings, and patents.
8. Demonstrate professional ethics and values by solving engineering problems for the benifite of the industry and society.

1. **Project Identification** - Idea Screening, Project Appraisal, Project Selection. Perform a literature search to review current knowledge and developments in the chosen technical area.

2. **Project Planning/Development of Project Network** - Work Breakdown Structure, Project Scheduling, Project Scheduling with Probabilistic Activity Times, Resource Considerations in Projects.

3**. Implementation Methodology** - Undertake detailed technical work in the chosen area using one or more of theoretical studies, computer simulations and hardware development.

4. **Results Analysis and Discussion** - Formulate the results obtained and discuss comparative analysis of secure results.

5. **Conclusion and Future Directions** - Prepare a formal report describing the work undertaken and results obtained so far; and Present the work in a forum involving poster presentations and demonstrations of operational hardware and software.

INTERNSHIP-III (after semester VI, summer internship)

Sr No	Items	Type of Internship to be undertaken
1	**Nature of Internship**	Industry / R and D labs / Education institutes (HEI less than 100 NIRFrank) This should be decided by the nature of Project-I selected by the group of students in the 5th semester. A project guide should assist in grooming the student group in relevant areas to enhance their knowledge and skills.
2	**End Semester Evaluation process**	Individual student / Group of students shall submit a report followed by viva voce by the department level faculty members on the project report prepared by them. A template for report writing and evaluation format will be provided by the Nodal Officer, COEP Tech.

Multi Disciplinary Minor (MDM) - BIS Standards for AI

Artificial Intelligence - Basic Concepts

Teaching Scheme
Lectures: 3 hrs./week
Practical: N/A

Examination Scheme
MSE - 30 marks
ESE - 50 marks
Internal - 20

Course Outcomes:

At the end of the course, students will demonstrate the ability to

1. Understand Basic Concept of AI
2. Analyze importance of Standards in AI

Unit 1 **(6 hrs)**

Introduction to AI

State Space Search

Water Jug Problem

Missionaries and Canibals Problem

BFS

Unit 2 **(6 hrs)**

Best First Search

A Star Search

And or Graph

Constraints Satisfaction Problem

Minimax Search

Alpha Beta Cut Off

Unit 3 **(6 hrs)**

Introduction to Knowledge Representation

Knowledge Agent

Predicate Knowledge

Introduction to Rule Based System

Forward and Backward Chaining

Unit 4 **(6 hrs)**

HMM Model

Conceptual Dependency

Semantic Network

Resolution Principal

DST

Unit 5 **(6 hrs)**

Introduction to Machine Learning

Supervised learning

Unsupervised Learning

Evolution of Algo

Need and Justification of Expert Systems

NLP

Unit 6 **(6 hrs)**

Introduction to Prolog
List in Prolog
Recursion in Prolog
Union and Intersection in Prolog
Parsing in AI

Semester VI: Challenges for standards formation in AI

(4 credits)

- Levels of automation in AI systems
- AI is software systems – why is necessity of standards
- AI specific risk and challenges
- AI systems –Role of standards
- Case studies: explore the scope of standards in AI systems